IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Original) A bipolar transistor comprising:

a substrate;

a intrinsic base region having a silicon buffer layer comprised of silicon which is formed on said substrate, and a composition-ratio graded base layer which is formed on the silicon buffer layer and comprises silicon and at least germanium and where a composition ratio of the germanium to the silicon varies in a thickness direction of the composition-ratio graded base layer; and

an extrinsic base region having an extrinsic base formation layer comprised of silicon which is formed on said substrate and adjacent to the silicon buffer layer;

wherein each of the extrinsic base formation layer and the silicon buffer layer has a thickness of not less than 40nm and a surface of the extrinsic base formation layer is silicided.

2. (Original) A bipolar transistor comprising:

a substrate;

a intrinsic base region having a silicon buffer layer comprised of silicon which is formed on said substrate, and a composition-ratio graded base layer which is formed on the silicon buffer layer and comprises silicon and at least germanium and where a composition ratio of the germanium to the silicon varies in a thickness direction of the composition-ratio graded base layer; and

an extrinsic base region having an extrinsic base formation layer comprised of silicon which is formed on said substrate and adjacent to the silicon buffer layer;

wherein a thickness of the extrinsic base formation layer is substantially equal to a thickness of the silicon buffer layer and a surface of the extrinsic base formation layer is silicided.

3. (Currently Amended) A bipolar transistor according to Claim 1 ~~or Claim 2~~, wherein the composition-ratio graded base layer is a silicon germanium graded base layer which comprises silicon and germanium.

4. (Currently Amended) A bipolar transistor according to Claim 1 ~~or Claim 2~~, wherein the silicon buffer layer is comprised of monocrystal and the extrinsic base formation layer is comprised of polycrystal.

5. (Original) A method of manufacturing a bipolar transistor comprising:

a step of forming a masking layer on a substrate to enclose a region including the active region;

a step of forming an epitaxial base layer such that the epitaxial base layer has a silicon layer and a silicon-germanium layer in the active region;

a step of, non-selectively with respect to the epitaxial base layer, forming a poly-base layer which comprises a silicon layer and a silicon-germanium layer in an isolation region of the region including the active region; and

a step of thereafter removing the silicon-germanium layer of the poly-base layer by etching process to expose a surface of the silicon layer as an extrinsic base formation layer, and

a step of forming a silicide layer on the exposed surface.

6. (Original) A method of manufacturing a bipolar transistor according to Claim 5, wherein the etching process is a wet etching which uses an etchant made of a mixture comprising nitric acid, water and fluorinated acid.

7. (New) A bipolar transistor according to Claim 2, wherein the composition-ratio graded base layer is a silicon germanium graded base layer which comprises silicon and germanium.

8. (New) A bipolar transistor according to Claim 2, wherein the silicon buffer layer is comprised of monocrystal and the extrinsic base formation layer is comprised of polycrystal.